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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/583,057	05/30/2000	Dale E Parson	3-2-1-4	1195

7590 05/10/2004

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EXAMINER	
BONURA, TIMOTHY M	
ART UNIT	**PAPER NUMBER**
2114	12

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/583,057	PARSON ET AL.	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 8-20* is/are rejected.

7)☒ Claim(s) *3 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-6, 8, 10, 12-13, 15-17, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adusumilli, U.S. Patent Number 6,385,749 and further in view of Key, U.S. Patent Number 6,173,386.

3. Regarding claim 1:

a. Regarding the limitation of "defining at least a subset of the processors as forming a group of processors to be subject to common control," Adusumilli discloses a system with a common controller for a group of multiple TAPs. (Lines 12-16 of Column 2).

b. Regarding the limitation of "delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group," Adusumilli teaches of a system with a multi-core processor with TAP controllers being controlled by a common interface controller. (Lines 12-16 of Column 2). Adusumilli also discloses group scan of the cells in the group. (Lines 25-35 of Column 5). Adusumilli does not disclose delaying the issuance of commands until a group scan is performed. Key discloses a multi-core processor system wherein a global fault signal is produced. Upon receiving this signal, the elements produce a signal that is sent back to the mail CPU to indicate the element for a transition to a debug mode. (Lines 11-21 of

Column 16). Key discloses that all of the components of the system are to enter the debug mode at the same time. (Lines 25-29 of Column 16). It would have been obvious to one of ordinary skill at the time of the invention to combine the common control of TAPs of Adusumilli and the delay of commands of Key. One of ordinary skill would have been inclined to combine the art because Adusumilli discloses that the TAP controllers generates status and test signal in response to these signals. (Lines 43-44 of Column 2). Thereby Adusumilli states a need to wait for the test signals. Key discloses that the synchronous entering of a debug mode, which the elements data information is to be, interrogated for facilitation debug operations. (Lines 55-57 of Column 16).

4. Regarding claim 2, Key discloses a system wherein the CPU provides information to the coprocessor to indicate elements in transition. (Lines 21-25 of Column 16).

5. Regarding claim 4, Adusumilli discloses a system with the IEEE 1149.1 standard. (Lines 8-9 of Column 60.

6. Regarding claim 5, Adusumilli discloses a system wherein a TAP performs a scan path. (Lines 25-36 of Column 5).

7. Regarding claim 6, Adusumilli discloses a system wherein the TAP is a member of common interface. (Lines 12-16 of Column 2).

8. Regarding claim 8, Key discloses a system wherein all of the Processing elements are similar in function. (Lines 15-24 of Column 10).

9. Regarding claim 10, Key discloses a system wherein all of the Processing elements are similar in function. (Lines 15-24 of Column 10).

10. Regarding claim 12, it is inherent to the JTAG specification that group scans are supplied as a serial stream of bits.

11. Regarding claim 13:

c. Regarding the limitation of "a chain manager operative to defining at least a subset of the processors as forming a group of processors to be subject to common control," Adusumilli discloses a system with a circuit control arrangement including a common controller for controlling a group of multiple TAPs. (Lines 12-16 of Column 2).

d. Regarding the limitation of "delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group," Adusumilli teaches of a system with a multi-core processor with TAP controllers being controlled by a common interface controller. (Lines 12-16 of Column 2). Adusumilli also discloses group scan of the cells in the group. (Lines 25-35 of Column 5). Adusumilli does not disclose delaying the issuance of commands until a group scan is performed. Key discloses a multi-core processor system wherein a global fault signal is produced. Upon receiving this signal, the elements produce a signal that is sent back to the mail CPU to indicate the element for a transition to a debug mode. (Lines 11-21 of Column 16). Key discloses that all of the components of the system are to enter the debug mode at the same time. (Lines 25-29 of Column 16). It would have been obvious to one of ordinary skill at the time of the invention to combine the common control of TAPs of Adusumilli and the delay of commands of Key. One of ordinary skill would have been inclined to combine the art because Adusumilli discloses that the TAP controllers generates status and test signal in response to these signals. (Lines 43-44 of

Column 2). Thereby Adusumilli states a need to wait for the test signals. Key discloses that the synchronous entering of a debug mode, which the elements data information is to be, interrogated for facilitation debug operations. (Lines 55-57 of Column 16).

12. Regarding claim 15:

e. Regarding the limitation of "a debugger," Key discloses a system with a debugger. (Lines 34-36 of Column 15).

f. Regarding the limitation of "a scheduler coupled to the debugger and operative to generate in response to signals from the debugger a set of debug commands for the processors," Keys discloses a system a remote processor which can control execution of debug features of the processor. (Lines 54-64 of Column 15).

g. Regarding the limitation of "a chain manager operative to defining at least a subset of the processors as forming a group of processors to be subject to common control," Adusumilli discloses a system with a circuit control arrangement including a common controller for controlling a group of multiple TAPs. (Lines 12-16 of Column 2).

h. Regarding the limitation of "receive one or more of the test commands for each of the processors in the group," Adusumilli discloses that the TAP controller has the ability to generates status and test signal and receive indication signals (Lines 51-56 of Column 2).

i. Regarding the limitation of "delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group," Adusumilli teaches of a system with a multi-core processor with TAP controllers being controlled by a common interface controller. (Lines 12-16 of Column 2). Adusumilli

also discloses group scan of the cells in the group. (Lines 25-35 of Column 5). Adusumilli does not disclose delaying the issuance of commands until a group scan is performed. Key discloses a multi-core processor system wherein a global fault signal is produced. Upon receiving this signal, the elements produce a signal that is sent back to the mail CPU to indicate the element for a transition to a debug mode. (Lines 11-21 of Column 16). Key discloses that all of the components of the system are to enter the debug mode at the same time. (Lines 25-29 of Column 16). It would have been obvious to one of ordinary skill at the time of the invention to combine the common control of TAPs of Adusumilli and the delay of commands of Key. One of ordinary skill would have been inclined to combine the art because Adusumilli discloses that the TAP controllers generates status and test signal in response to these signals. (Lines 43-44 of Column 2). Thereby Adusumilli states a need to wait for the test signals. Key discloses that the synchronous entering of a debug mode, which the elements data information is to be, interrogated for facilitation debug operations. (Lines 55-57 of Column 16).

13. Regarding claim 16, Adusumilli discloses a system wherein test signals are generated respective to each of the multiple TAP controllers. (Lines 65-67 of Column 2).

14. Regarding claim 17, it is inherent to the JTAG specification that group scans are supplied as a serial stream of bits.

15. Regarding claim 19:

j. Regarding the limitation of "define at least a subset of the processors as forming a group of processors to be subject to common control," Adusumilli discloses a system with a common controller for a group of multiple TAPs. (Lines 12-16 of Column 2).

k. Regarding the limitation of "receive one or more of the test commands for each of the processors in the group," Adusumilli discloses that the TAP controller has the ability to generates status and test signal and receive indication signals (Lines 51-56 of Column 2).

l. Regarding the limitation of "delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group," Adusumilli teaches of a system with a multi-core processor with TAP controllers being controlled by a common interface controller. (Lines 12-16 of Column 2). Adusumilli also discloses group scan of the cells in the group. (Lines 25-35 of Column 5). Adusumilli does not disclose delaying the issuance of commands until a group scan is performed. Key discloses a multi-core processor system wherein a global fault signal is produced. Upon receiving this signal, the elements produce a signal that is sent back to the mail CPU to indicate the element for a transition to a debug mode. (Lines 11-21 of Column 16). Key discloses that all of the components of the system are to enter the debug mode at the same time. (Lines 25-29 of Column 16). It would have been obvious to one of ordinary skill at the time of the invention to combine the common control of TAPs of Adusumilli and the delay of commands of Key. One of ordinary skill would have been inclined to combine the art because Adusumilli discloses that the TAP controllers generates status and test signal in response to these signals. (Lines 43-44 of Column 2). Thereby Adusumilli states a need to wait for the test signals. Key discloses that the synchronous entering of a debug mode, which the elements data information is to be, interrogated for facilitation debug operations. (Lines 55-57 of Column 16).

16. Regarding claim 20:

m. Regarding the limitation of "a chain manager operative to defining at least a subset of the processors as forming a group of processors to be subject to common control," Adusumilli discloses a system with a circuit control arrangement including a common controller for controlling a group of multiple TAPs. (Lines 12-16 of Column 2).

n. Regarding the limitation of "receive one or more of the test commands for each of the processors in the group," Adusumilli discloses that the TAP controller has the ability to generates status and test signal and receive indication signals (Lines 51-56 of Column 2).

o. Regarding the limitation of "delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group," Adusumilli teaches of a system with a multi-core processor with TAP controllers being controlled by a common interface controller. (Lines 12-16 of Column 2). Adusumilli also discloses group scan of the cells in the group. (Lines 25-35 of Column 5). Adusumilli does not disclose delaying the issuance of commands until a group scan is performed. Key discloses a multi-core processor system wherein a global fault signal is produced. Upon receiving this signal, the elements produce a signal that is sent back to the mail CPU to indicate the element for a transition to a debug mode. (Lines 11-21 of Column 16). Key discloses that all of the components of the system are to enter the debug mode at the same time. (Lines 25-29 of Column 16). It would have been obvious to one of ordinary skill at the time of the invention to combine the common control of TAPs of Adusumilli and the delay of commands of Key. One of ordinary skill would

have been inclined to combine the art because Adusumilli discloses that the TAP controllers generates status and test signal in response to these signals. (Lines 43-44 of Column 2). Thereby Adusumilli states a need to wait for the test signals. Key discloses that the synchronous entering of a debug mode, which the elements data information is to be, interrogated for facilitation debug operations. (Lines 55-57 of Column 16).

17. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key and Adusumilli as applied to claims 8 and 10 respectively above, and further in view of IEEE 1149.1 Specification.

18. Regarding claim 9, the IEEE specification states that the TAP controller is a synchronous finite state machine. (Top of Page 5-1). It would have been obvious to one of ordinary skill in the art at the time of the invention that since Adusumilli and Key follow the 1149.1 spec that this feature is inherent.

19. Regarding claim 11, the IEEE specification states that the TAP controller is a synchronous finite state machine. (Top of Page 5-1). It would have been obvious to one of ordinary skill in the art at the time of the invention that since Adusumilli and Key follow the 1149.1 spec that this feature is inherent.

20. Claims 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key and Adusumilli as applied to claims 13 and 15 respectively above, and further in view of Ritchie, U.S. Patent Number 4,135,240.

21. Regarding claim 14, Adusumilli and Key teach of a TAP controller system that can delay issuance of commands until groups scan of elements has been complete. They, however do not disclose that they chain manager can be implemented in software. Ritchie disclose that software

and hardware implementation are the same. (Lines 49-53 of Column 5). It would have been obvious to one of ordinary skill in the art at the time of the invention that such an implementation can be expressed in terms of either a computer program or a computer circuitry implementation, the two being functional equivalents of one another. (Lines 49-53 of Column 5).

22. Regarding claim 18, Adusumilli and Key teach of a TAP controller system that can delay issuance of commands until groups scan of elements has been complete. They, however do not disclose that they chain manager can be implemented in software. Ritchie disclose that software and hardware implementation are the same. (Lines 49-53 of Column 5). It would have been obvious to one of ordinary skill in the art at the time of the invention that such an implementation can be expressed in terms of either a computer program or a computer circuitry implementation, the two being functional equivalents of one another. (Lines 49-53 of Column 5).

Allowable Subject Matter

23. Claims 3 and 7 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

24. In view of the Appeal Brief filed on 2/20/2004, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth above.

25. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

26. If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 7:30-5:00, every other Friday off**. The examiner can be reached at: **703-305-7762**.

28. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Rob Beausoliel.**

- The supervisor can be reached on **703-305-9713.**

29. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

31. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **703-305-3900.**

32. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

  Alexandria, VA 22313-1450

Tim Bonura
Examiner
Art Unit 2114

tmb
May 4, 2004

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
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